CLMPTO
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1. A process for planarizing an integrated circuit structure comprising at least one dielectric layer on a silicon substrate, said dielectric layer having openings therein lined with a layer of electrically conductive barrier material and filled with copper filler material, said process consisting essentially of:

a) removing, by a chemical mechanical polish (CMP) process step, a portion of the excess copper filler material over the portion of an electrically conductive barrier layer lying on the upper surface of said dielectric layer;

b) removing, by an electropolishing process step, the remainder of said excess copper filler material over said portion of said electrically conductive barrier layer lying on said upper surface of said dielectric layer to thereby expose said underlying electrically conductive barrier layer on said upper surface of said dielectric layer; and

c) then removing exposed portions of said electrically conductive barrier layer on said upper surface of said dielectric layer in a dry etch reactor using a plasma etching process selective to said copper and said dielectric layer until all of said portions of said electrically conductive barrier layer over said upper surface of said dielectric layer are removed;

whereby said integrated circuit structure may be planarized by removal of all of said copper layer and said electrically conductive barrier layer from said upper surface of said dielectric layer while inhibiting dishing and/or erosion of the surface of said copper filler material in said openings dielectric layer.

2. The process of claim 1 wherein the amount of copper removed by said chemical mechanical polish (CMP) process step to remove sufficient excess copper (formed over the barrier liner portions on the top surface of the dielectric layer) to provide a planarized layer of excess copper with a global planarity of about 20 nm to about 30 nm.

3. The process of claim 2 wherein said dielectric layer comprises a layer of low k dielectric material.

4. The process of claim 2 wherein said silicon substrate, having said dielectric layer thereon, said barrier liner over said dielectric layer, and said excess copper thereon to be removed by said electropolishing process step, is immersed in an electrolytic bath of chemical reagents.

5. The process of claim 4 wherein said silicon substrate having said dielectric layer thereon, said barrier liner over said dielectric layer, and said excess copper thereon to be removed by said electropolishing process, is electrically connected to the positive electrode (anode) of a DC power supply.

6. The process of claim 5 wherein a counter electrode is also mounted in said electrolytic bath and said counter electrode is electrically connected to the negative electrode of said DC power supply.

7. The process of claim 6 wherein said DC power supply is capable of providing a DC voltage range of from about 0.5 volts DC to about 5 volts DC.

8. The process of claim 7 wherein said excess copper is removed from said barrier liner on said surface of said dielectric layer by said electropolishing process during a period of from about 10 seconds to about 10 minutes while maintaining, between said silicon substrate and said counter electrode, a DC potential ranging from about 0.5 volts to about 5 volts

9. The process of claim 7 wherein said excess copper is removed from said barrier liner on said surface of said dielectric layer by said electropolishing process during a period of from about 10 seconds to about 5 minutes while maintaining, between said silicon substrate and said counter electrode, a DC potential ranging from about 0.5 volts to about 5 volts.

10. The process of claim 2 wherein, after removal of said excess copper, said barrier liner is removed from said upper surface of said dielectric layer by contacting said exposed portions of said barrier liner, in a dry etch reactor, with a plasma ignited while flowing through said dry etch reactor one or more gases selected from the group consisting of Cl_2, CF_4, SF_6, C_4F_8, and BCl_3.

11. The process of claim 10 wherein said plasma is maintained at a power level ranging from about 5 watts to about 1500 watts.

12. The process of claim 11 wherein said reactor is maintained within a pressure range of from about 3 millitorr to about 1000 millitorr during said dry etch process.

13. The process of claim 12 wherein the temperature of said integrated circuit substrate is at least about -50°C during said dry etching process.

14. The process of claim 12 wherein the temperature of said integrated circuit substrate does not exceed about 200°C during said dry etching process.

15. The process of claim 10 wherein said etching of said barrier liner material is monitored monochromatically to determine the endpoint when all of the barrier liner material on the top surface of said dielectric layer has been removed.

16. A process for planarizing an integrated circuit structure comprising at least one low k dielectric layer on a silicon substrate having openings therein comprising vias and trenches lined with a layer of electrically conductive barrier liner material and filled with copper filler material which process comprises:

a) removing, by a chemical mechanical polish (CMP) first process step, a portion of the excess copper filler material over the portion of an electrically conductive barrier layer lying on the upper surface of said low k dielectric layer;

b) removing, by an electropolishing second process step, the remainder of said excess copper filler material over said portion of said electrically conductive barrier layer lying on said upper surface of said low k dielectric layer, b:

i) immersing said silicon substrate in an electrolytic bath;

ii) electrically connecting said silicon substrate to the positive electrode (anode) of a DC power supply;

iii) electrically connecting a counter electrode in said electrolytic bath to the negative electrode of said DC power supply to commence said electropolishing process; and

iv) maintaining, between said silicon substrate and said counter electrode, a DC potential ranging from about 0.5 volts to about 5 volts for a period of from about 10 seconds to about 10 minutes to thereby remove the remainder of said copper over said barrier line on the top surface of said low k dielectric layer, and to expose said underlying electrically conductive barrier layer on said upper surface of said low k dielectric layer; and

c) then removing, in a dry etch reactor, exposed portions of said electrically conductive barrier layer on said upper surface of said dielectric layer in a third plasma etching process step selective to said copper and said dielectric layer until all of said portions of said electrically conductive barrier layer over said upper surface of said dielectric layer are removed, said plasma etching step further comprising:

i) contacting said exposed portions of said barrier liner, in said dry etch reactor, with a plasma ignited while flowing through said dry etch reactor one or more gases selected from the group consisting of Cl_2, CF_4, SF_6, C_4F_8, and BCl_3. while maintaining said plasma at a power level ranging from about 5 watts to about 1500 watts, and said reactor within a pressure range of from about 3 millitorr to about 1000 millitorr, and a temperature of at least about -50°C but not exceeding about 200°C during said dry etching process; and

ii) monitoring said etching of said barrier liner material to determine the endpoint when all of said barrier liner material on the top surface of said dielectric layer has been removed.

CLAIMS 17-47. (CANCELLED)